WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a first sense amplifier which has a first terminal and a second terminal, compares an electric potential of said first terminal with an electric potential of said second terminal, and outputs an amplified voltage to each of said first and second terminals in accordance with a result of said comparison;

a second sense amplifier which has a third terminal and a fourth terminal, compares an electric potential of said third terminal with an electric potential of said fourth terminal, and outputs an amplified voltage to each of said third and fourth terminals in accordance with a result of said comparison;

a first bit line which is connected to said first terminal and belongs to a first area;

a second bit line which is connected to said second terminal and belongs to a second area which does not overlap with said first area;

a third bit line which is connected to said third terminal and belongs to said first area;

a fourth bit line which is connected to said fourth terminal and belongs to said second area;

a first memory cell which is connected to said first bit line and has a ferroelectric capacitor;

a first dummy memory cell which is connected to said second bit line and has a ferroelectric capacitor polarized to a first direction;

a second memory cell which is connected to said third bit

line and has a ferroelectric capacitor;

a second dummy memory cell which is connected to said fourth bit line and has a ferroelectric capacitor polarized to a second direction opposite to said first direction; and

first short-circuit means which can short-circuit said second and fourth bit lines.

2. A memory according to claim 1, wherein said short-circuit means short-circuits said second and fourth bit lines after information is read out from both of said dummy memory cells to the corresponding bit lines.

3. A memory according to claim 1, wherein polarizing directions of both of said ferroelectric capacitors of said first and second dummy memory cells are sequentially reversed every after completion of a reading operation of data from said first memory cell by an operation of said first sense amplifier.

4. A memory according to claim 1, further comprising:

a third dummy memory cell which is connected to said first bit line and has a ferroelectric capacitor polarized to a third direction;

a third memory cell which is connected to said second bit line and has a ferroelectric capacitor;

a fourth dummy memory cell which is connected to said third bit line and has a ferroelectric capacitor polarized to a fourth direction opposite to said third direction;

a fourth memory cell which is connected to said fourth bit line and has a ferroelectric capacitor; and

a second short-circuit means which can short-circuit said first and third bit lines.

5. A driving method of a semiconductor memory, comprising:

a first step of reading out information stored in a first memory cell and inducing a first electric potential onto a first bit line;

a second step of reading out stored information from a first dummy memory cell having a ferroelectric capacitor polarized to a first direction and inducing a second electric potential onto a second bit line;

a third step of reading out stored information from a second dummy memory cell having a ferroelectric capacitor polarized to a second direction opposite to said first direction and inducing a fourth electric potential onto a fourth bit line;

a fourth step of short-circuiting said second and fourth bit lines by first short-circuit means after said third step;

a fifth step of releasing said short-circuited second and fourth bit lines; and

a sixth step of activating a first sense amplifier, comparing an electric potential of said first bit line with an electric potential of said second bit line and outputting an amplified voltage to each of said first and second bit lines in accordance with a result of said comparison.

6. A method according to claim 5, further comprising:

a seventh step of writing predetermined information into said first dummy memory cell so that the ferroelectric capacitor which

said first dummy memory cell has is polarized to said second direction; and

an eighth step of writing predetermined information into said second dummy memory cell so that the ferroelectric capacitor which said second dummy memory cell has is polarized to said first direction,

and wherein said seventh and eighth steps are executed after said sixth step.

7. A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which can be connected to a first bit line through a switching device;

a sense amplifier comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell;

first and second dummy memory cells having ferroelectric capacitors which can be connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are mutually polarized to opposite directions as storage information in the dummy memory cells, when the data is read out, the operation to apply the electric potentials from both of said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually

electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by said short-circuit of both of said second and third bit lines by said short-circuit means is supplied as a reference potential to said sense amplifier.

8. A memory according to claim 7, wherein the polarizing directions of said ferroelectric capacitors of both of said dummy memory cells are sequentially reversed to the opposite directions every said data reading.

9. A semiconductor memory comprising:

a memory cell having ferroelectric capacitor which can be connected to a first bit line through a switching device;

a sense amplifier comparing an electric potential of said first bit line with a reference potential in order to read out data in said memory cell;

first and second dummy memory cells having ferroelectric capacitors which can be connected to a second bit line and a third bit line through switching devices in order to apply said reference potential to said sense amplifier; and

short-circuit means which short-circuits said second and third bit lines at the time of said data reading,

wherein said ferroelectric capacitors of both of said dummy memory cells are mutually polarized to opposite directions as storage information in the dummy memory cells, and each time the data is read out, the polarizing directions of said ferroelectric capacitors of both of

said dummy memory cells are sequentially reversed to the opposite directions.

10. A memory according to claim 9, wherein an intermediate value of both electric potentials of said bit lines which are applied from said ferroelectric capacitors of both of said dummy memory cells to each of said bit lines corresponding thereto is supplied as a reference potential to said sense amplifier.

11. A memory according to claim 9, wherein the operation to apply the electric potentials from both of said dummy memory cells to each bit line corresponding thereto is executed in a state where both of said second and third bit lines are mutually electrically shut off, and thereafter, an intermediate value of both electric potentials of both of said second and third bit lines which is obtained by the short-circuit of both of said second and third bit lines by said short-circuit means is supplied as a reference potential to said sense amplifier.